21. (Previously Presented) The computer readable medium of Claim 19, wherein said method further comprises determining that a data path exists from said first data controller to said second data controller through a path including said first and second external data interfaces.

22. (Original) The computer readable medium of Claim 19, wherein said method further comprises testing a plurality of data controllers using a single scan chain.

23. (Previously Presented) The computer readable medium of Claim 19, wherein said method further comprises performing an electrical connectivity test of a data path comprising said first external data interface and said second external data interface.

REMARKS

The claims remaining in the present application are Claims 1-23. Claims 1, 2, 3, 9, 10, 19, and 20 have been amended. No new matter has been added as a result of these amendments.

Claim Objection

Claim 3 was objected to due to an informality. Claim 3 has been amended to remove the informality.

35 U.S.C. §102

Claims 1-3, 6, 8-10, 15-17, 19-21 and 23 are rejected under 35 U.S.C. §102(e) as being anticipated by Nejedlo et al., U.S. Published Patent Application 2004/0117709

(hereinafter, Nejedlo). The rejection to Claims 1-3, 6, 8-10, 15-17, 19-21 and 23 is respectfully traversed for the reasons below.

Currently Amended Claim 1 recites, in part:

> transferring a test pattern from within said electronic device, said test pattern transferred between a first data controller coupled to a first external data interface of said electronic device and a second data controller coupled to a second external data interface of said electronic device via an element external to said device and coupling said first and second external data interfaces, wherein said first external data interface and said second external data interface are not typically coupled together externally during operation of said electronic device

Independent Claims 9 and 19 contain similar limitations to those of Claim 1. Claims 2 – 8 depend from Claim 1 and add further limitations to the claimed invention. Claims 10-18 depend from independent Claim 9 and add further limitation to the claimed invention. Claims 20-23 depend from independent Claim 19 and add further limitations to the Claimed invention.

Applicant submits that Nejedlo does not teach or suggest, either expressly or inherently, the limitation of transferring a test pattern from within said electronic device, said test pattern transferred between a first data controller coupled to a first external data interface of said electronic device and a second data controller coupled to a second external data interface of said electronic device via an element external to said device and coupling said first and second external data interfaces, wherein said first external data interface and said second external data interface are not typically coupled together externally during operation of said electronic device, as recited in Claim 1. Nejedlo teaches generating a test pattern for testing either the internal busses in an electronic device or for the testing of the interconnects in a single board; see e.g.,

paragraph 21, Figure 1a, Figure 1b, board 580, and busses 10, 20, 30, 40, 50, 510, and 540 of Nejedlo. However, Nejedlo is silent with regard to several of the limitations recited in Claim 1. Firstly, Nejedlo is silent with respect to an external element for coupling a first and second external interfaces together. Secondly, Nejedlo is silent with respect to coupling external interfaces externally to one another, let alone coupling external interfaces to one another that are not typically externally coupled during normal operation. Thirdly, Nejedlo is silent with respect to generating a test pattern within the electronic device, and then sending it out of the electronic device through one external interface, and finally receiving it back into the electronic device through a second external interface.

Therefore, Applicants respectfully submit that Nejedlo fails to anticipate the Applicants' invention as is set forth in Claims 1, 9, and 19, and as such, Claims 1, 9 and 19, overcome the rejection under 35 U.S.C. 102(e), and Applicants submit these claims are in condition for allowance. Accordingly, the Applicants also respectfully submit that Nejedlo does not anticipate or render obvious the embodiments of the claimed invention as recited in Claim 2-8 dependent on Claim 1, Claims 10-18 dependent on Claim 9, or Claims 20-23 dependent on Claim 19, and that these Claims overcome the rejection under 35 U.S.C. 102(e) through dependency on allowable base claims.

35 U.S.C. §103

Claims 4-5 and 11-12

Claims 4-5 and 11-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nejedlo in view of Marchevsky, U.S. Patent No. 6,572,384

(hereinafter, Marchevsky). Applicants have reviewed the cited references, and respectfully submit that the embodiments of the present invention as recited in Claims 4, 5, 11, and 12 are neither anticipated nor rendered obvious by Nejedlo in view of Marchevsky, either alone or in combination. Independent Claims 1 and 9 recite similar limitations. Claims 4 and 5 depend from independent Claim 1 and recite further limitations to the claimed invention. Claims 11 and 12 depend from independent Claim 9 and recite further limitations to the claimed invention.

Marchevsky discloses a single form factor that can support many subsystem designs on a personal computer (see e.g., col. 6 lines 32-47 of Marchevsky), however, Marchevsky is silent regarding transferring a test pattern over external data interfaces, regardless of whether the form factors of the external interfaces are the same or different. Further, Marchevsky does not cure the deficiencies noted above with Nejedlo with respect to independent Claims 1 and 9. Specifically, Marchevsky, like Nejedlo, is silent with respect to an external element for coupling a first and second external interfaces together. Secondly, Marchevsky, like Nejedlo, is silent with respect to coupling separate external interfaces externally to one another, let alone coupling external interfaces to one another that are not typically externally coupled during normal operation. Thirdly, Marchevsky, like Nejedlo, is silent with respect to generating a test pattern within the electronic device, and then sending it out of the electronic device through one external interface, and finally receiving it back into the electronic device through a second external interface.

Therefore, Applicants respectfully submit that the combination of Nejedlo and Marchevsky fails to anticipate the Applicants' invention as is set forth in Claims 1, 4, 5, 9,

11, and 12, and as such, Claims 1, 4, 5, 9, 11, and 12 overcome the rejection under 35 U.S.C. 103(a), and Applicants submit these claims are in condition for allowance. Accordingly, the Applicants also respectfully submit that the combination of Nejedlo and Marchevsky does not anticipate or render obvious the embodiments of the claimed invention as recited in Claim 4 and 5 dependent on Claim 1 or Claims 10 and 11 dependent on Claim 9 and that Claims 4, 5, 10, and 11 overcome the rejections under 35 U.S.C. 103(a) through dependency on allowable base claims.

Claims 7, 18 and 22

Claims 7, 18 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nejedlo in view of Rajski, U.S. Patent No. 5,991,898 (hereinafter, Rajski). Applicants have reviewed the cited references, and respectfully submit that the embodiments of the present invention as recited in Claims 7, 18, and 22 are neither anticipated nor rendered obvious by Nejedlo in view of Rajski, either alone or in combination. Independent Claims 1, 9, and 19 recite similar limitations, as do dependent claims 7, 18, and 22. Claim 7 depends from independent Claim 1 and recites further limitations to the claimed invention. Claim 18 depends from independent Claim 9 and recites further limitations to the claimed invention. Claim 22 depends from independent Claim 19 and recites further limitations to the claimed invention.

Rajski discloses an arithmetic built-in self-test of multiple scan-based integrated circuits, see e.g., col. 3 line 65 – col. 4 line 42 or Rajski. However, Rajski is silent regarding transferring a test pattern over external data interfaces, as Rajski is

entirely devoted to scanning done within an integrated circuit, see e.g., Figure 1 item 10, and col. 5 lines 29-49 of Rajski. Further, Rajski does not cure the deficiencies noted above with Nejedlo with respect to independent Claims 1, 9, and 19. Specifically, Rajski, like Nejedlo, is silent with respect to an external element for coupling a first and second external interfaces together. Secondly, Rajski, like Nejedlo, is silent with respect to coupling separate external interfaces externally to one another, let alone coupling external interfaces to one another that are not typically externally coupled during normal operation. Thirdly, Rajski, like Nejedlo, is silent with respect to generating a test pattern within the electronic device, and then sending it out of the electronic device through one external interface, and finally receiving it back into the electronic device through a second external interface.

Therefore, Applicants respectfully submit that the combination of Nejedlo and Rajski fails to anticipate the Applicants' invention as is set forth in Claims 1, 7, 9, 18, and 19, and 22, and as such, Claims 1, 7, 9, 18, and 19, and 22 overcome the rejection under 35 U.S.C. 103(a), and Applicants submit these claims are in condition for allowance. Accordingly, the Applicants also respectfully submit that the combination of Nejedlo and Rajski does not anticipate or render obvious the embodiments of the claimed invention as recited in Claim 7 dependent on Claim 1, Claim 18 dependent on Claim 9, or Claim 22 dependent on Claim 19, and that Claims 7, 18, and 22 overcome the rejections under 35 U.S.C. 103(a) through dependency on allowable base claims.

Claims 13-14

Claims 13-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nejedlo in view of Allen, U.S. Patent No. 6,237,048 (hereinafter, Allen). Applicants have reviewed the cited references, and respectfully submit that the embodiments of the present invention as recited in Claims 13 and 14 are neither anticipated nor rendered obvious by Nejedlo in view of Allen, either alone or in combination. Claims 13 and 14 depend from independent Claim 9 and recites further limitations to the claimed invention.

Allen discloses jumper switches that can be used within a single PCI (Peripheral Component Interconnect) card (see e.g., Figure 1, and Col 4, lines 45-65 of Allen), rather than a card that can be used as a jumper, as recited in Claims 13 and 14. In fact, Allen is silent with respect to either a first element or a second element comprising a plug in PCI jumper card adapted to be inserted into a PCI card slot, as recited in Claims 13 and 14. Further, Allen does not cure the deficiencies noted above with Nejedlo with respect to independent Claim 9. Specifically, Allen, like Nejedlo, is silent with respect to an external element for coupling a first and second external interfaces together. Secondly, Allen, like Nejedlo, is silent with respect to coupling separate external interfaces externally to one another, let alone coupling external interfaces to one another that are not typically externally coupled during normal operation. Thirdly, Allen, like Nejedlo, is silent with respect to generating a test pattern within the electronic device, and then sending it out of the electronic device through one external interface, and finally receiving it back into the electronic device through a second external interface.

Therefore, Applicants respectfully submit that the combination of Nejedlo and Allen fails to anticipate the Applicants' invention as is set forth in Claims 9, 13 and 14, and as such, Claims 9, 13, and 14 overcome the rejection under 35 U.S.C. 103(a), and Applicants submit these claims are in condition for allowance. Accordingly, the Applicants also respectfully submit that the combination of Nejedlo and Allen does not anticipate or render obvious the embodiments of the claimed invention as recited in Claims 13 and 14 dependent on Claim 9, and that Claims 13 and 14 overcome the rejections under 35 U.S.C. 103(a) through dependency on allowable base claims.

SUMMARY

In view of the foregoing remarks, the Applicants respectfully submit that the pending claims in the instant patent application are in condition for allowance. The Applicants respectfully request reconsideration of the Application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact the Applicants' designated representative at the below listed phone number.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

Dated: 8/23, 2005

James P. Hao
Registration No. 36,398

Address: WAGNER, MURABITO & HAO LLP
Two North Market Street
Third Floor
San Jose, California 95113

Telephone: (408) 938-9060 Voice
(408) 938-9069 Facsimile